

In the Specification:

Page 1, paragraph 1:

The present application is a continuation-in-part of, and claims priority from, [U.S. Patent Application Serial] Application No. 09/664,121 filed September 18, 2000, and still pending.

Page 1, paragraph 2:

[Technical Field] Background of the Invention

This invention relates to the field of heat sink and heat spreader structures and, more particularly, to heat sink/spreader structures which utilize thermoelectric effects to more efficiently dissipate thermal energy from electronic devices including Integrated Circuit (IC) devices and their associated packaging.

Page 1, paragraph 3:

[Background of the Invention] Description of the Related Art

The performance levels of microelectronic devices (e.g., integrated circuits, power amplifiers) are continually increasing to keep pace with the demands of modern technology. Performance levels such as clock speed are closely tied to the number and density of features (e.g., transistors) patterned onto the microelectronic device. Faster processing by the microelectronic device demands faster clock speeds. Faster clock speeds, in turn, mean more switching and power dissipation per unit time.

Page 4, paragraph 6:

U.S. Pat. No. 4,646,126, granted to Lizuka on February 24, 1987 relates to [a] multiple IC chips mounted to a separate silicon substrate (via an oxide layer) and wiring layers interconnecting them.

Page 6, paragraph 2:

U. S. Pat. No. 4,698,662, granted to Young, et al. on October 6, 1987 relates to a multichip module [is] in which IC chips are dielectrically bonded to a silicon substrate which, in turn, is dielectrically bonded to a heat sink. Electrical conductive traces are deposited onto the substrate's surface to provide electrical connection between the chips and package pins.

Page 8, paragraph 2:

One object of the present invention is to provide a heat dissipating IC device structure in which the silicon substrate itself is part of a thermoelectric couple, which may have an external electric potential applied.

Page 10, paragraph 2:

FIGS. 5a through 5c illustrate one method of fabricating thermoelement couples onto an IC device substrate.

Page 10, paragraph 3:

FIGS. 6a through 6e illustrate another method of fabricating the present invention.

Page 10, last paragraph:

[Best mode for Carrying Out the Invention] Detailed Description of the Invention

Described below are several embodiments of the present invention which illustrate various ways the present invention can be implemented. In the descriptions that follow, like numerals represent like elements in all figures. For example, where the numeral 10 is used to refer to a particular element in one figure, the numeral 10 appearing in any other figure refers to the same element.

In the Drawings:

Applicant includes sheets showing the proposed drawing changes in red (submitted with previous amendment version).